RESEARCH ARTICLE   OPEN ACCESS

Bit Error Rate Testers-A Study

Lakshmy Sukumaran, Dharani. K.G
Student, MVJ College of Engineering Bangalore
Assistant Professor, MVJ College of Engineering Bangalore

Abstract
This paper is a comparative study of the various BERT (bit error rate testers), which are used widely for measuring the performance of any digital communication systems.
Keywords—BERT; Monte Carlo (MC); IS (importance sampling); software based BERT; hardware based BERT; FPGA based BERT;

I. INTRODUCTION

Any digital transmission system which transmits a series of bits over a communication channel is likely to introduce some errors due to various factors like noise, interference etc. We need to ensure that these errors are reduced to a minimum so as not to interfere with the working of the communication system and maintain its data integrity. To ensure such behaviour it is essential that we carry out specific measurements of BER on the test system. BER is a measure of how effective the system is and indicates the number of bit error introduced in the received message. BER Testers are used to measure this value and this paper provides a comparative study of the various types of BER Testers available.

II. WHAT IS BER?

With the increasing demand for short design cycles in the rapidly expanding field of wireless digital communications, developing a reliable system scalable to various emerging new standards and technology is quite a challenge. One way to accomplish this is to reduce the testing time and to get the testing done at an earlier stage of design so as to minimize the amount of reworks that would be required later. So we go for testing at the earliest possible stage, PHY layer or baseband layer. One such widely used performance metric at the physical layer which effectively identifies the reliability of a wireless communication link (right from bits input to the bits out through the entire antenna sub system, signal path and channel) is Bit Error Rate. In simple terms, it is defined as the number of bits in error to the total number of transmitted bits, measured over the fixed interval of time. A strong signal with an undisturbed path will result in a very negligible value of BER. Thus BER becomes significant when the signal traverses through a rapidly changing disturbing channel. The BER analysis is usually done theoretically using the mathematical analysis.[1],[2].

Although the concept of determining the bit error rate-sending a known sequence through the channel and comparing the received signal against the known sample to keep a count of the errors- is simple, the execution suffers a setback. One method is the pseudorandom method where we use the pseudorandom data sequence for transmission. We call this pseudo since it is not exactly possible to model a random data transmission over a channel, accurately and completely using the mathematical models. Another one is the practical approach wherein we need to install the complete communication systems we intend to test, including the antenna, entire radio, in the actual or laboratory created environment. It is a highly impractical and time consuming costly solution.[2]

There are mainly two methods employed to measure the bit error rate. One is the software based simulations like Monte Carlo simulations (MC) or Importance sampling (IS).The other one is the hardware based prototyping. [3]

III. SOFTWARE BASED SIMULATIONS

Although in theory it is possible to obtain a closed form expression for the bit error rate using the various available mathematical analyses, it is practically impossible. A more pragmatic approach needs to be taken which can be applied even when the analytical description of the system is unavailable.

A) Monte Carlo(MC)

One such practical approach is the software based Monte Carlo simulations. Monte Carlo simulations ,detecting an error is treated a success. For a range of input sequences defined by probability distribution functions, MC estimator has to estimate the probability of error. [3]

B) The Importance Sampling (IS):

 C) The IS approach is an improvement over the MC process in such a way to alter the properties of statistical processes involved in the MC technique to the point of improving the chances of success. It employs the variance reduction technique by the use of a unbiased estimator which modifies the original distribution and hence reduce the variance of the BER estimate calculated for a range of inputs.[3]

The various problems encountered with the software based simulations are given in the following section.

- If the noise introduced by the channel is extremely less, the errors introduced are less and hence it can be considered as a reliable transmission. So a larger time must be required for the simulations in order to receive a desired level of BER set. That indicates the time for the simulations depends on the set BER that we need to verify implying that the time needed for the BER estimate will be a function of BER itself. For example, the MC simulation requires at least 100/Pe experiments (where Pe is the desired BER) to yield an estimator with relative precision of 10% This makes the MC simulation method highly inappropriate for systems with very low BER.[4]

- The performance of a wireless system depends a great deal on the characteristics of the radio channel .In the laboratory test environment, these channels are replicated using fading channel simulators. The disadvantages of this equipment is that it is very costly in terms of half a million dollars or so.It cannot however be scaled up to provide the requirements of emerging new wireless systems.The commercially available fading channel simulators along with some of their chracteristics have been given in table1 below.[1],[5]

TABLE I. COMMERCIALLY AVAILABLE FADING CHANNEL SIMULATORS

Fading channel simulators	No of channels	No of paths per channel	Maximum Doppler (HZ)	Maximum Delay spread(msec)	Baseband bandwidth (Mhz)
ARC Smartsim [6]	64	36	2777	-	20
ACE 400 NB[7]	32	18	6	0.0012	20
PROP sim C8[8]	16	48	22000	6.4	50
N5115A [9]	2	48	2400	10	15
R&S ABFS [10]	2	12	1600	1.6	5
NJB-1600B [11]	2	12	800	0.2	10
SR_550 [12]	2	24	2000	2	13
Sofi05 [13]	2	24	4000	25	8

- For complex communication systems with computationally intensive systems like the MIMO, the software based MC simulations of baseband layer is extremely time consuming and costly. As an example, a wireless system should perform over various radio channel characteristics like AWGN, fading channel, indoor or outdoor environments etc. Also all the available operating modes should also be tested like the 300odd modulation schemes and coding available in 802.11 standards etc. Thus a wide variety of possible configurations need to be explored before arriving at the optimum one, for systems like MIMO. This makes the software simulations a computationally daunting process, thus providing a hindrance to timely design verification.[1]

- The BER measurement of wireless systems over different channels differs. It is a relatively simpler process to do MC based simulation for BER analysis on a AWGN channel compared to the fading channels, where the error performance needs to be averaged not only over independent instances of noise and data (like we do for a AWGN channel)but over fading channel samples as well, over a longer duration.[14]

- The bit error rate of any reliable communication link should be very low. For example in the IEEE 802.3 10 GB/sec Ethernet , it should be of

the order of 10^{-12} for it to be termed as reliable. This indicates that a very large number of symbols need to be processed for software based simulators, over different SNR ratios to obtain a reliable performance measurement .Thus the simulation time can get extended to months .The time required to estimate the BER reliably is directly proportional to the target minimum number of error at each operating point and inversely proportional to erfc ($10 ^ (E_b /N_0)$).[15]

$$T= [2N_e]/[R_b* erfc (10^ \{Eb/20 *No\}] \quad \ldots\ldots(1)$$

Where

N_e is the target minimum number of error at an operating point.

R_b-number of samples per second, i.e. the bit rate erfc- complementary Gaussian error function integral (E_b /N_0)- signal to noise ratio in db.

No - The one sided spectral density.

E_b- Energy per received bit

From the above equation (1), it can be inferred that the simulation time increases exponentially with magnitude of the signal to noise ratio.[15][16]

IV. HARDWARE BASED BERT

The accurate BER measurements can be obtained by observing the performance in the test field .This calls for a very extensive and expensive test set up. Also carrying out the over the air experiments with a large number of possible configurations makes it a very difficult approach. So we go for a more practical approach, hardware based prototyping at the baseband.[1][16]

The hardware based simulators accelerate the performance compared to software simulators. But the available commercial test equipment has the following drawbacks

- They are not scalable to keep pace with the emerging new standards and technology, as new configurations may need to be tested.
- The available BERT can be used only at a later stage, typically at the RF stage after the fabrication of the system.
- New custom interfaces may have to be designed to connect the device under test to the BERT, which could add to the design burden.

The available BER testers in the market has been compiled and presented in the below sections.

- Tektronix offers a wide range of Bit Error Rate Testers for bit error rate analysis of the device under test thus reducing the product development cycle.[17]

TABLE II. COMMERCIALLY AVAILABLE BERT FROM TEKTRONIX[17]

Product Series	Maximum bit rate(Gb/sec)	Channels
BitAnalyser BA series	1.5-1.6	1
BERTscope BSA series	8.5-28.6	1
Patternpro@PPGseries	12.5-40	1,2,4
Patternpro@PEDseries	32-40	1,2

- Another bit error rate tester from DCB (Data Communication for Business Inc) is the 120V ac powered BT-1 RS-232 Bit Error Rate Test Set BERT. The BT-1 is an excellent bench test or field testing tool. Applications involves in locating problems in polling systems, multiplexer systems, carrier communications, wireless systems, and more.[18]
- Picosecond Pulse Labs, which has been now acquired by the Tektronix, has the new and improved 32Gb/s PAM-4 BERT system.[19]
- Absolute Analysis Investigator™ Bit Error Rate Tester (BERT) supports multiple speeds from 1Gbps to 4Gbps, and generates test patterns for fiber channel, Ethernet, FPDP, and many other physical layers.It can detect Bit error rates upto 10^{-12} and supports 32 ports for testing.[20]
- Another one is from LUCEO Technologies providing the X-BERT and Parallel X and 14g parallel BERT systems.[21]

Most of the published hardware based BERT uses the FPGA (Field Programmable Gate Array) and tools like SIMULINK to integrate various FEC (forward error correction) blocks onto FPGA. The logic of FPGA is held either in look up tables, registers, multiplexers, distributed or blocks memory. In addition to these FPGA have dedicated circuitry for speedy calculations, high speed input output circuitry and embedded processors. The memory bandwidth of n FPGA is also highly commendable. These two features of FPGA-high speed parallel ALU and memory bandwidth- enables FPGA as a potential candidate for implementing the various data path algorithms. The FPGA usage limited by the lack of familiarity with the hardware designs, FPGA and languages like Verilog, HDL.[17]

Even though using the system tools like SIMULINK eliminates the need for having a good knowledge of the hardware, it poses some disadvantages [15]

- The simulation library may have only limited resources like various communication blocks. It may not have blocks which could cater to new emerging technology standards.

- The available designs do not have the flexibility in architecture for adding, removing a module.
- The Gaussian noise can be generated using analog components, which lacks accuracy and could be used only for specific circumstances. The other method is the generation of psuedonoise using the digital components, which is more flexible and widely used. Most of the published BERT utilizes an inaccurate model for GNG (Gaussian Noise Generator), reducing the reliability of BER measurements

So we go for a more complete solution offered by implementing all of the digital communication processing modules like the encoder, modulator, decoder, demodulator along with the fading channel and the AWGN channel onto a single FPGA, providing a repeatable test environment. It has been observed that the FPGA based BERT increases cost effectiveness by reducing the testing cost than the one done using commercial test equipment and channel simulators. Also such FPGA based BERT increases productivity as time required for these, when compared with software based simulations, is very less. It also provides flexibility.[15]

V. CONCLUSION

A comparative study of the various BER Testers was performed and it is deferred that FPGA based BERT is a step ahead than its contemporaries, in terms of speed and flexibility. Hardware-accelerated validation is essential to speed up the characterization of computationally intensive and rapidly evolving modern wireless communication systems.

REFERENCES

[1]   A. Alimohammad, S. F. Fard, and B. F. Cockburn, "FPGA-based accelerator for the verification of leading-edge wireless systems," in Proc. IEEE Int. DAC, Jul. 2009, pp. 844–847.

[2]   Breed, G. (2003, January). Bit Error Rate: Fundamental concepts and measurement issues. Retrieved April 07, 2014, from high frequency electronics: http://www.high frequencyelectronics.com/Archives/Jan03/HFE0103_Tutorial.pdf[

[3]   Bohdanowicz, A. (n.d.). On Efficient BER Evaluation of Digital Communication Systems via Importance Sampling. Retrieved April 07, 2014, from CiteSeerx: http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.118.2785&rep=rep1&type=pdf

[4]   Peter J. Smith, Mansoor Sha_ and Hongsheng Gao, \Quick sim-ulation: A review of importance sampling techniques in communication systems," IEEE Journal on Selected Areas in Communications, vol. 15, pp. 597{613, May 1997.

[5]   A. Alimohammad, S. F. Fard, and B. F. Cockburn, "FPGA-accelerated baseband design and verification of broadband MIMO wireless systems,"in Proc. IEEE 1st Int. Conf. Adv. Syst. Testing Validation, Sep. 2009,pp. 135–140.

[6]   ARC Seibersdorf Research GmbH, Vienna, Austria.MIMO Channel Simulator, 2007.

[7]   Azimuth Systems Inc., Acton, MA, USA. ACE 400NB MIMO Channel Emulator, 2006.

[8]   Elektrobit Inc., Oulunsalo, Finland. Multi-Channel Emulator, EB Propsim C8, 2008.

[9]   Technical Overview, N5115A, Agilent Technologies Inc. Baseband Studio for Fading, 2005.

[10]   Data sheet, Rohde & Schwarz.

[11]   Baseband FadingSimulator ABFS, Saving costs through baseband simulation, 2004.Product Manual, NJZ-1600B, Japan Radio Co.Multipath Fading Simulator, 2005.

[12]   Technical Document, SR5500, Spirent Communications. Wireless Channel Emulator, 2006.

[13]   Sofimation, Helsinki, Finland. SOFI05 Radio Channel Simulator, 2006.

[14]   A. Alimohammad, S. F. Fard,. "FPGA-Based Bit Error Rate Performance Measurement of Wireless Systems"in. IEEE Transactions on VLSI systems. DOI10.1109/TVLSI.2013.2276010

[15]   A. Alimohammad, S. F. Fard, and B. F. Cockburn, "Hardware-based error rate testing of digital baseband communication systems," in Proc.IEEE ITC, Oct. 2008, pp. 1–10.

[16]   V. Singh, A. Root, E. Hemphill, N. Shirazi, and J. Hwang, "Accelerating bit error rate testing using a system level design tool," in Proc. 11th Annu. IEEE Symp. FCCM, Apr. 2003, pp. 62–68.

[17]   Inc, T. (n.d.). Bit error rate tester. Retrieved April 07, 2014, from tektronix inc: http://in.tek.com/bit-error-rate-tester

[18]   CB. (n.d.). Datasheet. Retrieved April 07, 2014, from DCB: http://www.dcbnet.com/datasheet/bt1.html?gclid=CKKw-4jdxr0CFcwipQodgWIA_g

[19]   Picosecond Pulse Labs, I. (2013, August). PICOSECOND PULSE LABS ANNOUNCES NEW 32GB/S PAM-4 BERT SYSTEM. Retrieved April 07, 2014, from Picosecond Pulse Labs: http://www.picosecond.com/about/content.asp?spid=133

[20]   Absolute Analysis, I. (n.d.). Bit error rate tester. Retrieved April 7, 2014, from Absolute analysis: ttp://www.absoluteanalysis.com/solutions/by-products/bit-error-rate-tester.html

[21]   Inc, L. (n.d.). 14G single channel and parallel testing for 16GFC, Infiniband FDR, QSFP, AOC, CFP, CXP and more. Retrieved April 07, 2014, from Luceotec: http://www.luceotec.com/